APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,918	05/23/2002	Kazuo Sekiya	JP920010014US1	4408

877 7590 02/27/2004		

IBM CORPORATION, T.J. WATSON RESEARCH CENTER
P.O. BOX 218
YORKTOWN HEIGHTS, NY 10598

EXAMINER
WARD, AARON S

ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 02/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _23 May 2002_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-17_ is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-17_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _23 May 2002_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a)☒ All   b)☐ Some * c)☐ None of:

   1.☒ Certified copies of the priority documents have been received.

   2.☐ Certified copies of the priority documents have been received in Application No. _____.

   3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
   application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1.   The information disclosure statement filed June 21, 2002 fails to comply with 37 CFR

1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently

understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the

content of the information, of each patent listed that is not in the English language. It has been

placed in the application file, but the information referred to therein has not been considered.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3.   Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Hartman et al.

(U.S. Patent No. 5,495,265).

As to claim 1, Hartman et al. teaches an LCD including a cell 2-5 (Fig. 1) forming a

display area, a driver 22 applying a voltage, and an overdrive controller 10 – 21 to apply

overdrive voltage exceeding a target value (column 5, lines 30-33). The overdrive controller 10

– 21 stores predicted capacitance values and calculates overdrive voltage based on predicte4d

capacitance (column 6, lines 17-25).

As to claim 2, the LCD includes a memory 20 storing voltage information for capacitances. The overdrive controller 10 – 21 interpolates (column 2, lines 36-56) the voltage information stored in memory 20 to calculate the overdrive voltage.

As to claim 3, the overdrive controller 10 – 21 predicts a capacitance value (column 2, line s 36-48) of a pixel 4 one frame period later (column 4, lines 7-12 "subsequent") when applying a predetermined voltage to the pixel 4 with a certain capacitance value and stores the prediction (column 2, lines 47-55).

As to claim 4, the LCD further includes memory 20 storing capacitance values of pixels 4 reached on frame period later (column 4, lines 7-12 "subsequent") when applying predetermined voltage to the pixel 4 with a certain capacitance value. The overdrive controller 10 – 21 interpolates the information (column 2, lines 36-48) about the stored capacitances in the memory 20 to calculate the predicted value.

As to claim 5, the cell 2 – 5 has a nature where brightness change delays compared with capacitance change (column 1, lines 51-64).

As to claim 6, Hartman et al. teaches an LCD including cell 2 – 5 displaying an image from pixels 4 having a TFT structure (column 4, line 2), a driver 22 applying voltage to each pixel 4 of the cell 2 – 5, and controller 10 – 21 controlling the driver 22 to apply voltage exceeding applied voltage (column 5 lines 30-33) when displaying brightness on the cell. The controller 10 – 21 includes voltage calculating means (column 2 lines 47 – 48) for calculating cell voltage based on brightness on refresh cycle later (column 4, lines 7-12 "subsequent") corresponding to displayed pixel value and present capacitance of the pixel predicted in advance (column 6, lines 17-25).

As to claim 7, the controller 10 – 21 includes capacitance predicting means (column 2, lines 47-48 and column 6, lines 17-25) for predicting pixel capacitance value reached after the refresh cycle when applying the calculated voltage with the present capacitance, and storage means 20 (column 6, lines 19-20) for storing predicted capacitance values. The voltage calculating means (column 2, lines 47-48) and capacitance predicting means predicts based on stored capacitance values (column 6, lines 17-46).

As to claim 8, the LCD includes a memory 20 storing information to obtain voltage from present capacitance value and capacitance value information a pixel 4 will reach when applying voltage to the pixel 4 with a predetermined capacitance (column 2, lines 47-48 and column 6, lines 17-25).

As to claim 9, the stored information in memory 20 used to obtain voltage and capacitance are discrete simulated values (column 2, lines 51-56).

As to claim 10, the stored information in memory 20 used to obtain voltage and capacitance are obtained from transition from a static state (column 1, lines 58-61).

As to claim 11, Hartman et al. teaches an LCD drive circuit include capacitance predicting means (column 6, lines 17-42) where each pixel 4 reaches one refresh cycle later (column 4, lines 7-12 "subsequent") when applying predetermined targeted voltage/brightness, storage means 20 for storing predicted capacitance, and voltage calculating means (column 2, lines 47-48) for each pixel 4 voltage based on brightness one refresh cycle later and stored capacitance.

As to claim 12, the capacitance predicting means (column 6, lines 17-42) reads predetermined information from memory 20 that stores capacitance information obtained at one

refresh cycle later (column 4, lines 7-12 "subsequent") when applying predetermined pixel 4

voltage with certain capacitance, and interpolates (column 2, lines 36-48) the read informationg

to predict the capacitance value.

As to claim 13, the voltage calculating means (column 2, lines 47-48) reads

predetermined information from memory 20 for obtaining applied voltage from certain

capacitance value, and interpolates (column 2, lines 36-48) the read information based on stored

capacitance value in storage 20 to calculate applied voltage.

As to claim 14, Hartman et al. teaches a method wherein an input pixel 4 value is

overdriven (column 5, lines 30-33) to output a modified value including predicting capacitance

value each pixel 4 will reach one refresh cycle later (column 4, lines 7-12 "subsequent") when

applying a predetermined voltage for input pixel value, storing the predicted capacitance

(column 6, lines 19-20), and calculating an overdrive voltage (column 6, lines 20-42) to each

pixel 4 based on input value one refresh cycle later (column 4, lines 7-12 "subsequent") and the

stored capacitance.

As to claim 15, the overdrive voltage is calculated (column 6, lines 17-42) using stored

capacitance value as a start point and target pixel brightness one refresh cycle later (column 4,

lines 7-12 "subsequent").

As to claim 16, Hartman et al. teaches a method for driving an LCD wherein brightness

change delays relative to capacitance change (column 1, lines 51-64), including predicting pixel

capacitance value when applying predetermined voltage (column 2, lines 36-46), calculating

voltage exceeding target pixel value based on input target using predicted capacitance value

(column 5, lines 30-33), and supplying predetermined voltage to the LCD based on calculated

voltage (column 6, lines 4-7).

As to claim 17, Hartman et al. teaches a program for directing a computer 1 (Fig. 1) to

drive an LCD 2 – 6, including predicting capacitancewhere each pixel will reach one refresh

cycle later (column 4, lines 7-12 "subsequent") when applying predetermined voltage to the LCD

(column 6, lines 16-46), storing the predicted capacitance in buffer 20 of the computer 1, and

calculating applied pixel voltage based on pixel value one refresh cycle later and stored

capacitance value (column 4, lines 7-12 "subsequent").

Conclusion

4.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure.

Johnson et al. (6,304,254) is directed to a display device for overdriving pixels.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Aaron S. Ward whose telephone number is (703) 305-8992. The

examiner can normally be reached on Monday - Friday, 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Steven J. Saras can be reached on (703) 305-9720. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ASW

STEVEN SARAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600